4 WAFER FABRICATION EQUIPMENT

(Shaded Material is Unreleased)

1.0.0 WAFER FABRICATION EQUIPMENT

Wafer fabrication equipment consists of all those types of equipment used in making and processing raw wafers in forming the finished chips—whether they be discretes or integrated circuits. This segment also includes mask making. However, by convention, it excludes both test and assembly of the finished product.

The wafer fabrication equipment market comprises roughly 50% of the total equipment market for all of semiconductor manufacturing. Exact percentages of the total segment and its subsegments will be found in the database sections of each of the following chapters.

As a point of reference, historical sales and bookings are shown in Figure 4.0.0-1. The wafer processing equipment market reached an all-time peak in sales during the year 1985. Annual sales for 1985 were $3.2B. However, the great recession of 1985 had already set in, so much of 1985's success was due to buying inertia carryover from 1984.

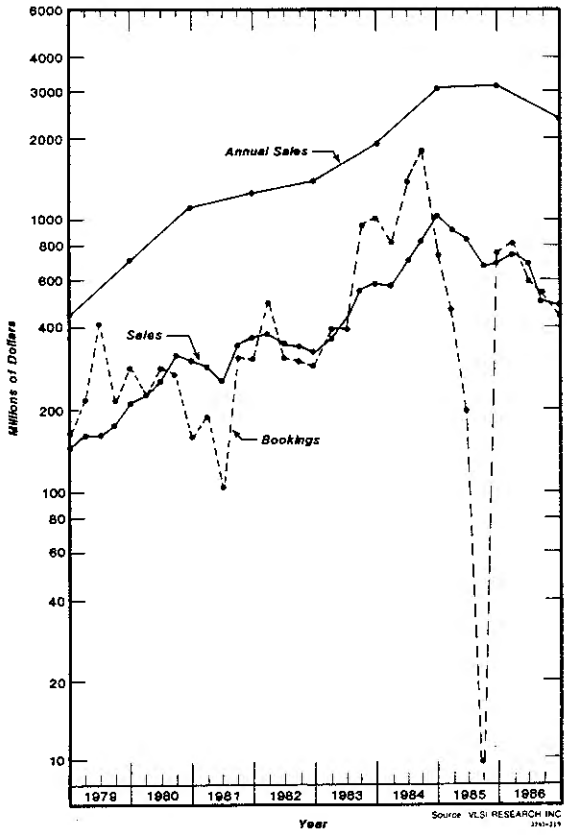

Figure 4.0.0-1

WAFER PROCESSING EQUIPMENT SALES AND BOOKINGS 1979-86

4.1 SEMICONDUCTOR WAFER FAB EQUIPMENT CHARACTERISTICS

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4.1.0 CURRENT SEMICONDUCTOR MANUFACTURING CHARACTERISTICS

At some time in the future when the final chapter of semiconductor manufacturing can be set down in writing, its author will likely point back to the period of the mid-eighties as a time of fundamental change in manufacturing. Not so much because of sophisticated new manufacturing methods such as automation, computer aided design, or computer integrated manufacturing—these are merely the outward manifestations of change; nor so much due to the massive competitive repositioning between the United States and Japan. Rather, that future author will likely point out the cause as being how the responsibility for processing know-how shifted from semiconductor manufacturers to their equipment suppliers during this time. Prior to the eighties, semiconductor manufacturers reigned supreme in their knowledge of processing. Equipment suppliers, by-and-large, acted merely as system integrators, often lacking detailed knowledge of how their equipment was put to use.

However, during this period of enormous change, the equipment manufacturers stepped up to the task of learning how their equipment contributed to the success—or lack of it—in semiconductor manufacturing. They experimented with all kinds of new methods for improving their equipment, as well as how to improve the basic manufacturing process. In so doing, they changed the face of manufacturing and simultaneously became the central storehouses of process knowledge. Semiconductor manufacturers became chip designers. This reversal of responsibilities was dramatically portrayed during the bring-up of Intel's infamous Fab 4 in Albuquerque, and the new NMB facility in Tokyo. Intel—on the one hand—represented the preeminent authority in integrated circuits. They built Fab 4 in opposition to the outspoken recommendations of their suppliers. It was a failure. NMB—on the other hand—was a newcomer, knowing nothing of semiconductor manufacturing, having been in the ball bearing business. NMB licensed the technology and used the processes developed by its equipment suppliers. Its line was made operational in record time, while Intel's languished.

4.1.1 Overall Development Of The Industry

4.1.1 Overall Development Of The Industry

The wafer fabrication equipment industry grew out of the enormous effort of the 1950s and the 1960s to perfect integrated circuits. By the late fifties, the semiconductor industry had turned its back on germanium as the basic raw material and was in hot pursuit of silicon instead. There were numerous reasons. Those same reasons which made silicon more appealing as a raw material contributed heavily to the growth of the equipment industry. A silicon oxide 'skin' could be grown over silicon, but not over germanium. This both protected or 'passivated' the silicon and simultaneously permitted selective etching. New equipment thus came into being to support both passivation and etching. Today's chemical deposition equipment markets, etching equipment markets, and microlithography equipment markets rely heavily upon that singular facet of silicon.

Silicon has a higher melting temperature than does germanium. This offered much greater operating ranges in hostile thermal environments. Higher manufacturing temperatures were required, where much greater diffusion sensitivities could be obtained. The diffusion equipment market flourished.

Today, the wafer fabrication market can be categorized by six major segments. Together, these six have some sixteen or more subsegments. Microlithography is a key process in wafer fabrication. Microlithography equipment capabilities, limitations, and cost have a great deal to say in determining requirements of all the other equipment. Consequently, it will be discussed first in the following sections.

Wafer Fabrication is the heart of semiconductor manufacturing. By our definition it begins with crystal growing and ends with a finished wafer that is ready to be die probed or wafer probed. That is, when each die is fully ready to be functionally tested.

A flow chart of a typical fabrication line is shown in Figure 4.1.1-1. This is the so-called front-end of a semiconductor line. Wafers first arrive from a wafer making company (such as Wacker or Monsanto). They are then scrubbed, cleaned and prepared for further processing in manners that are akin to those used in a hospital operating room. But the cleanliness used in semiconductor manufacturing makes a hospital operating room dirty by comparison. The entire front-end is maintained in a special area of the plant which has become known as the 'white room', under class 1 to class 10 clean room conditions. The name 'white room' is due partly to the bright lights and the stark white appearance. But the name is also used partly to differentiate the 'white room' from the so-called 'yellow room'. Microlithographic activities are conducted in the 'yellow room'. The yellow room area is by far the cleanest, the most delicate, and the most environmentally controlled portion of the entire manufacturing line.

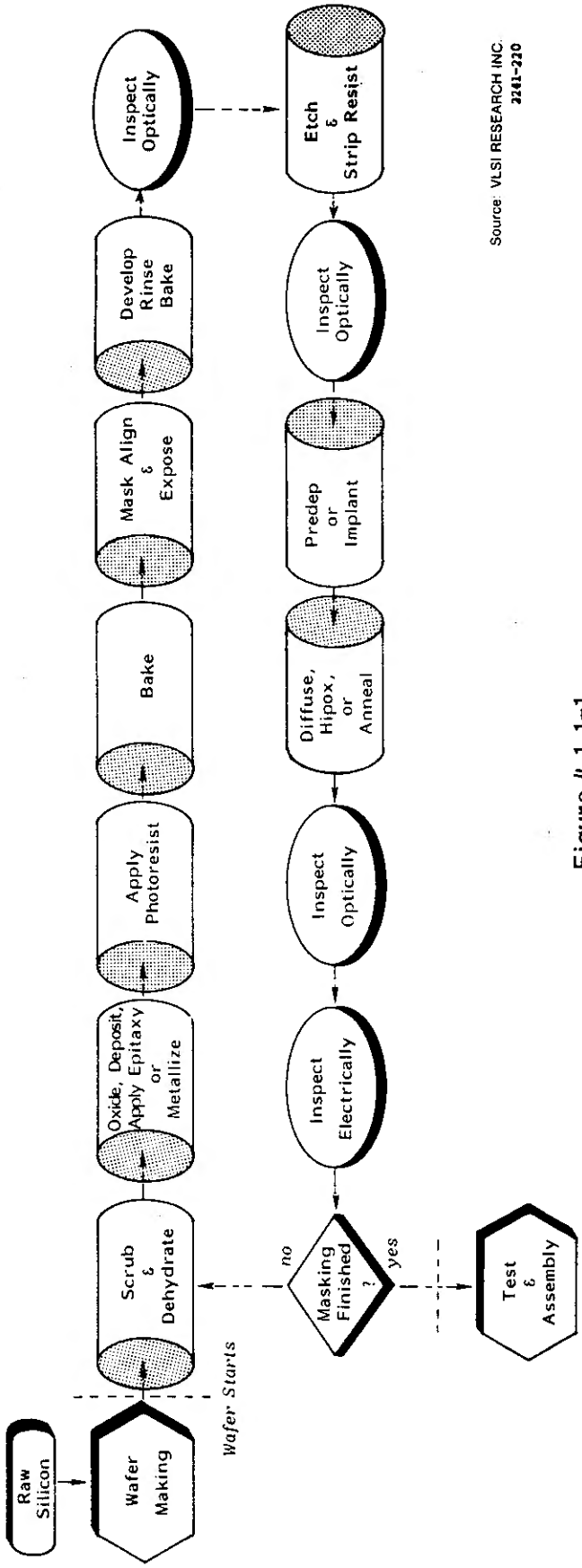


Figure 4.1.1-1

THE SEMICONDUCTOR WAFER FABRICATION PROCESS

The 'yellow room' is almost—but not quite—the innermost sanctum of a semiconductor manufacturer's plant. That is reserved for the mask design and layout process itself. Still, the yellow room supplies the heartbeat for the operation. In the early years, it was thought that only the lithography area need be so clean. In time it was discovered that the entire process required 'yellow room' class conditions.

As is well known, the wafer fabrication process consists of a series of steps. These are oxidation, deposition, masking, diffusion and implant. Each step is repeated from 5 to 12 times on every wafer to be processed. The actual steps were described in detail in Section 1.1.2. They are reported for a typical CMOS process diagram in Figure 4.1.1-2. For review, the wafer initially has an oxide grown over its surface. The oxide is then coated with a thin layer of light-sensitive material called photoresist. (Typical photoresist suppliers are Kodak, Shipley, Hunt Chemical and others.) A pattern of the circuit is then projected onto the photoresist. A wafer aligner is used to selectively expose the photoresist. The photoresist—or resist, as it is normally called—is then developed in a manner somewhat similar to that of a conventional photograph. Afterwards the resist is rinsed away in areas where light rays did not strike, leaving the underlying oxide coating completely exposed. These holes in the resist are called windows. Next the oxide covering the silicon is etched away at these windows, exposing the bare silicon beneath. The bare silicon in these windows is then doped via diffusion or implantation equipment.

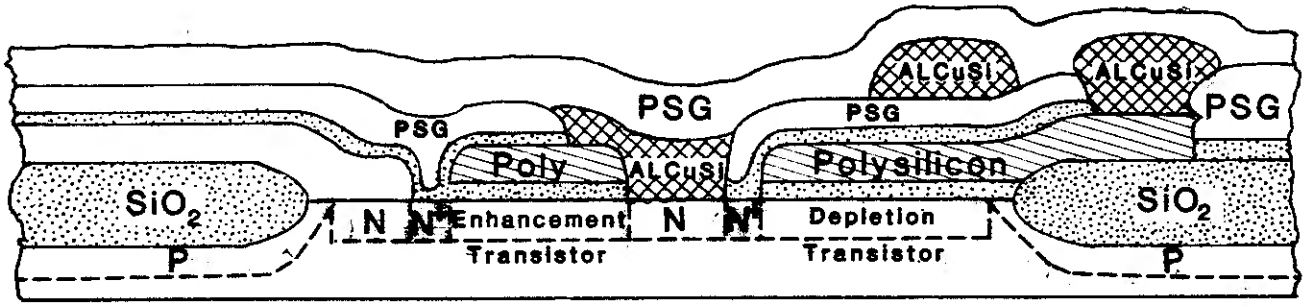
Two chemical dopants are typically used. One is boron, the other is phosphorus. They alter the silicon electrically, but in opposite directions of charge. The entire objective of the process is to obtain an extremely delicate balance between these oppositely charged materials; and then to be able to carefully upset the balance in a controlled and intentional manner. The method of control is to inject a few extra charged particles, via electrical currents, at the input connections of the integrated circuit.

This charge balance is so delicate, and the manufacturing and cleanliness requirements to achieve it are so demanding, that only a very few die ever make it out of manufacturing. Consequently, the equipment used tends to be extremely sophisticated. Each new breakthrough in manufacturing that achieves better yield and gets more die to the finish line results in still more complicated equipment. Yield is thus the engine which drives the equipment manufacturing market.

Equipment for this manufacturing is broken into six major categories, each of which is described at length in Sections 4.3 through 4.8. The six segments are listed in their entirety in Table 4.1.1-3.

Figure 4.1.1-2

Silicon Gate NMOS Manufacturing Steps



	Processing Step	Equipment Used	Material Used
1	Initial Oxidation	Diffusion Furnace	
2	Implant Barrier Deposition	LPCVD	Silicon Nitride
3	Field Oxide Mask	Aligner	Mask, Photoresist
4	Etch	Etcher	Acid, Gas
5	Field Implant	Ion Implanter	Boron
6	Field Oxidation	Diffusion Furnace	
7	Strip Nitride	Barrel Plasma	Gas
8	Depletion Transistor Mask	Aligner	Mask, Photoresist
9	Depletion Channel Implant	Ion Implanter	Phosphorus
10	Gate Oxidation	Diffusion Furnace	
11	Enhancement Transistor Mask	Aligner	Mask, Photoresist
12	Enhancement Transistor Implant	Ion Implanter	Boron
13	Buried Contact Mask	Aligner	Mask, Photoresist
14	Etch	Etcher	Acid, Gas
15	Polysilicon Deposition	LPCVD	Gas
16	Dope Polysilicon	Diffusion Furnace	Phosphorus
17	Source/Drain Mask	Aligner	Mask, Photoresist
18	Etch	Etcher	Acid, Gas
19	Source/Drain Implant	Ion Implanter	Arsenic
20	Dielectric Oxidation	Diffusion Furnace	
21	Contact Mask	Aligner	Mask, Photoresist
22	Etch	Etcher	Acid, Gas
23	Dielectric Deposition	Vapox	PSG
24	Reflow	Diffusion Furnace	
25	Etch	Etcher	Acid, Gas
26	Metal Deposition	Sputterer	AlCuSi, AlSi
27	Interconnect Mask	Aligner	Mask, Photoresist
28	Etch	Etcher	Acid, Gas
29	Passivation Deposition	Vapox	PSG
30	Bonding Pad Mask	Aligner	Mask, Photoresist
31	Etch	Etcher	Acid, Gas

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TABLE 4.1.1-3

OVERALL WAFER FABRICATION EQUIPMENT SEGMENTS

■ MICROLITHOGRAPHY ■

- Resist Processing Equipment
- Wafer Exposure Equipment
- Mask Making Equipment

■ DIFFUSION/OXIDATION ■

- Diffusion Furnaces
- Hi-Pox Systems
- Rapid Thermal Processing

■ ION IMPLANTATION ■

- Low to Medium Current
- High Current
- High Energy

■ DEPOSITION ■

- CVD — Chemical Vapor Deposition
- PVD — Physical Vapor Deposition
- EPI — Epitaxial Film Deposition

■ ETCHING & CLEANING ■

- Dry Etching and Cleaning
- Wet Etching and Cleaning

■ WAFER MANUFACTURING ■

- Crystal Growing Furnaces
- Crystal Machining

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4.1.2 Overall Technology Trends In Wafer Fabrication

4.1.2 Overall Technology Trends In Wafer Fabrication

Technology trends in wafer fab continue to be driven by productivity which is itself driven by yield factors. Opportunities for yield improvement are so pervasive they tend to permeate all aspects of equipment manufacturing. Almost invariably, however, the contributing factors in yield losses are contaminants. Contaminants may come from particulates outside the equipment; or they may be generated by the equipment itself; or they may come from redeposits of the process material during processing.

While yield can be a volume-dependent phenomenon, it is usually a surface-area-dependent phenomenon. For this reason, it is heavily affected by packing density. Packing density, in turn, is a most apparent restriction in memory devices. Consequently, from a device viewpoint, memory devices become the technology drivers.

Demand for memory devices has continued to be an important driving force within the industry and is expected to remain so for the indefinite future. Memory devices lead the industry in terms of both packing density and linewidth. This is because packing density is determined by linewidth. As was shown in Chapter 2, memory devices represent the technology state-of-the-art threshold and are well ahead of microprocessors or other types of devices. As will be shown further, 1M bit memory devices require about 1.25 micron linewidths in order to be fabricated, and these devices are fully packed, using vertical stacking and multiple metal layers in order to ease packing density constraints.

Further increases in memory size will require either still lower linewidths—well into the sub-micron region—or will require higher die size, or both. As has been repeatedly shown, aligners which allow higher yields—such as steppers—will permit larger die sizes without significant yield losses. Consequently, memories can be expected to bring even higher pressure for investment in stepping aligners in order to relax the need for tighter linewidths.

Memories are driving all other equipment markets as well. For example, smaller device geometries require greater diffusion control. Consequently, the market for computer controlled diffusion furnaces has been advanced by memory devices. Deposition is still another area affected by memories. Memories are bringing new epitaxy and plasma enhanced CVD applications to MOS manufacturing. The impact of memories upon dry etching equipment has been so pronounced and so well publicized that it should not need mentioning.

It has been shown frequently over the years that the lower limits of linewidths are decreasing exponentially with time. Figure 4.1.2-1 shows our interpretation of how this has been occurring. The narrowest linewidth that was needed on a production basis up through the 1950's

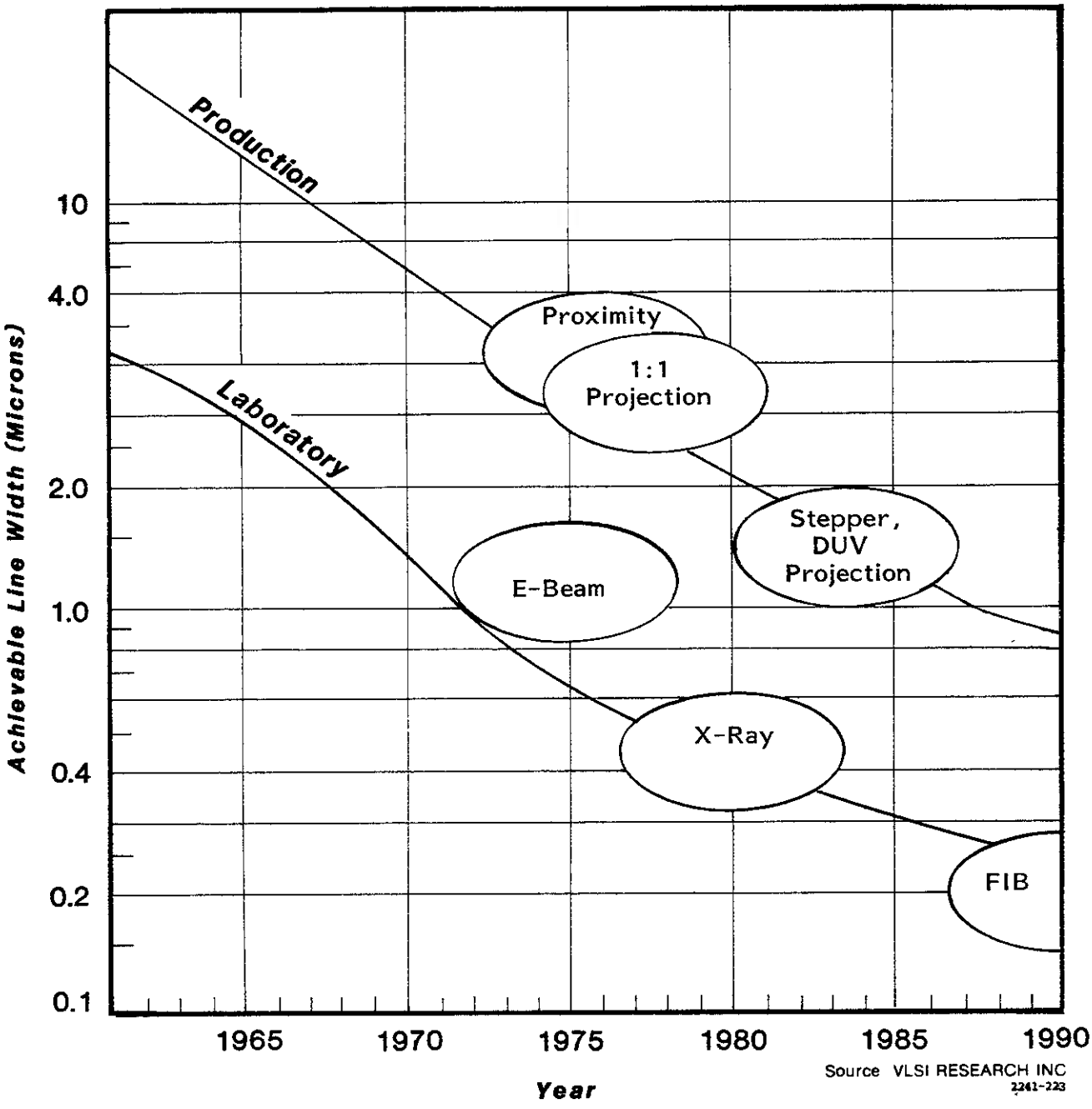

Figure 4.1.2-1

LINE WIDTH VERSUS TIME

and into the early 1960's was about 25 microns. Memory devices were introduced in the late sixties and packing densities began to rise excessively. By late 1979, most manufacturers were using the lower limits of 2 to 2.5 microns on advanced memory devices. They were pushing the state-of-the-art of equipment. Nonetheless, laboratory equipment is available that can reduce the linewidth still more. Such laboratory equipment remains too complicated for day-in, day-out manufacturing use. E-beam, deep UV proximity, and X-ray methods are available today for achieving sub-micron linewidths in laboratory and pilot line operations. Consequently, continued pressures are being brought to reach sub-micron dimensions.

Temperature effects have begun to arise throughout the fab line. This is partly due to the increased size of the wafers—there is greater runout error with larger wafers, such as with six inch or eight inch ones. But the decreased tolerance of temperature effects is also partly due to the smaller geometric dimensions in use—there now is much less room for error than before. A suitable manufacturing tolerance for one micron lines, made from several mask overlays, cannot exceed about 0.1 microns altogether.

High temperatures also cause wafer bowing and curling. This results in out-of-focus alignments. Most focus tolerances that can be achieved and held in practice, are about 0.6 microns. But worst-case temperature errors can cause as much as 1.2 micron change. Such out-of-focus conditions might cause a 1.0 micron line to become either short-circuited with the next line, or to completely vanish altogether! Consequently, there is immense pressure to reduce manufacturing temperatures. This in turn, is creating demand for new low temperature equipment. This issue is one of the driving forces for CVD equipment and for rapid thermal processing.

Chemical etching encounters difficulties at two micron dimensions as well. So too, does aluminum evaporation. Chemical etching undercuts the film. Aluminum evaporation has non-uniform patches of material and poor step coverage. The former is generating demand for plasma dry-etching equipment, the latter for sputtering equipment.

Material issues are also having an important effect. Parasitic resistance and capacitance are now limiting the ability of the industry to further scale-down device sizes. Materials have changed little since the early seventies.

The tremendous success of the stepping aligner is mitigating some of this pressure to reduce linewidths. It produces larger yielding die and permits larger die to be used. Consequently, larger geometries are being used as well.

The parameter called wafer starts is one of the more important determinants of demand for process equipment. Wafer starts is just the number of wafers started each week by a fab line. They directly determine the number of wafer passes that equipment is required to process each year. Table 4.1.2-2 depicts a three year summary of how wafer starts affected equipment demand in the years from 1983 to 1985. (See Section 1.3 for updated information.)

LSI and VLSI technologies drive the market for wafer fabrication equipment. In 1984, LSI technology generated more demand for new equipment than did either LSI or VLSI. Total LSI wafer starts reached 77.5 million. This was a 25.5 million increase in wafer starts over those of 1983. These new wafer starts generated demand for $1595M of new investment in fabrication equipment for LSI manufacturing. However, VLSI technology was generating the greater demand for new equipment by 1985. In 1984, new VLSI wafer starts generated demand for $1496M of new equipment investment.

Automation is an important structural change occurring in wafer processing. Automation was once defined as a concept of "Sand in—finished product out". However, this concept does not provide a realistic definition for a fully automated plant. Consequently, this idea faded as proponents learned that it crossed four major industry segments and an equal number of manufacturing sites spread half way around the world. Additionally, the "sand in—finished product out" concept tended to stress automation as being equivalent to mechanization. But industry rejected this notion as well, choosing instead to define automation as consisting of single-button 'smart' machines but not necessarily mechanization. Still, the idea helped to focus a good deal of attention upon just what automation is.

The semiconductor industry does not necessarily equate automation with non-manual operation—that is—the mere replacement of people with machines. Nor does it necessarily envision automation as consisting mainly of automated mechanisms for wafer transport and control. Instead, automation implies getting people out of sensitive manufacturing areas. This is because they are the major inhibitants to achieving high yielding lines. Automation also means 'smarter' machines, capable of operating themselves without a great amount of operator attendance. In other words, automated machines are simpler on the outside, more complex on the inside.

As mentioned, the main benefit of automation is improved productivity through process yield improvement. Presently, people are the major restraints in achieving high yielding lines. As is commonly known, people contribute some thirty percent of all contamination found in fab areas. Hence, one key objective and driving force within automation is to remove people from such sensitive manufacturing areas.

TABLE 4.1.2-2

WORLDWIDE WAFER FABRICATION EQUIPMENT DEMAND
(in millions of passes)

Item	1983					1984					1985				
	DISCRETE	SSI/MSI	LSI	VLSI	TOTAL	DISCRETE	SSI/MSI	LSI	VLSI	TOTAL	DISCRETE	SSI/MSI	LSI	VLSI	TOTAL
Wafer Starts (in millions of units)	11.4	59.1	52.0	21.4	143.9	11.2	86.9	77.5	35.7	211.3	10.9	79.2	84.7	51.6	226.4
MICROLITHOGRAPHY	94	672	996	556	2318	140	1018	1510	842	3510	164	1182	1752	978	4076
Resist Processing	47	336	498	278	1159	70	509	755	421	1755	82	591	876	489	2038
Alignment	47	336	498	278	1159	70	509	755	421	1755	82	591	876	489	2038
DIFFUSION	68	415	338	145	966	102	629	512	219	1462	119	730	594	255	1698
ION IMPLANT	31	127	246	137	541	50	210	425	233	918	59	247	516	279	1101
Medium Current	31	127	106	93	357	50	210	175	154	589	59	247	205	181	692
High Current	-	-	140	44	184	-	-	250	79	329	-	-	311	98	409
DEPOSITION	45	272	321	170	808	69	411	485	256	1221	79	478	563	298	1418
CVD	21	103	141	102	367	32	156	213	154	555	37	182	248	179	646
PVD	20	150	170	61	401	30	226	257	92	605	34	263	298	107	702
Epitaxy	4	19	10	7	40	7	29	15	10	61	8	33	17	12	70
ETCHING	225	1080	1979	773	4057	303	1795	2635	1146	5879	294	1636	2881	1651	6462
Strip	75	429	601	259	1364	101	695	775	393	1964	98	634	847	568	2147
Dry Etch	-	-	78	86	164	-	-	209	173	382	-	-	229	245	474
Wet Etch	75	296	520	171	1062	101	579	488	152	1320	98	527	534	219	1378
Wet Clean	75	355	780	257	1467	101	521	1163	428	2213	98	475	1271	619	2463

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There are two additional reasons for wanting people out. People cause process variations by making mistakes. Mistakes lead to non-uniform results and catastrophic accidents. One example is wafer inspection. Wafers inspected by humans exhibit as much as 400% variation between two different but equally well-trained operators. Numerous stories exist of wafers lots which have been lost by an operator. These lots inevitably show up at the wrong place and are then processed anyways. Automation can eliminate these human mistakes. At the same time, process reproducibility is improved.

Automation provides several other benefits, as well. Figure 4.1.2-3 depicts various items end users see as justification for automation. Two side-benefits often quoted are relief from trained labor shortages and for quick turnaround. As machines become more automated and more reliable, fewer trained personnel will be needed. In turn, current-day labor shortages may be alleviated altogether. However, the overall impact is still unclear. For example, some users fear that fewer workers may translate into more maintenance techs to keep the equipment operating. This would merely be an exchange of cheap labor for expensive labor. Consequently, labor is not viewed as a strong motivation for automation.

Quick turnaround, however, is viewed as an important element. In the past, sixteen to twenty weeks were needed for the processing of a product. Today, three to six weeks is more common. With full automation, processing time can be only a few days. For example, IBM's QTAT line does this in just three days.

The acronym 'QTAT' means Quick Turn-Around Time. It is part of an uncommitted logic array facility at IBM that processes only the last three masks. These are metalization masks.

IBM has solved both the downtime issue and the cleanliness issue with its QTAT system. The active areas of each module are enclosed in plastic. The wafer is thereby kept in a clean environment. In the original QTAT line—now shut down—the designed-for cleanliness was Class 50; Class 20 was actually seen by the wafer. Just outside the enclosure, the cleanliness level was Class 5000 on IBM's original line. Consequently, maintenance crews and assembly line workers were able to work within a few inches of a clean wafer without contaminating it. Moreover, because the 'tools' were in parallel, the plant was not brought down because any one tool was down.

The advantage to this is lower inventory with higher yield. It has been shown that for every day removed from work-in-process time, a 5% increase in yield occurs if total WIP time is around 12 days. This is depicted in Figure 4.1.2-4. This is an improvement which has proven elusive without some form of integrated factory control.

Figure 4.1.2-3

Justifications For Automation

(ratings on a scale of 1 to 10, 10 being important, 1 being unimportant)

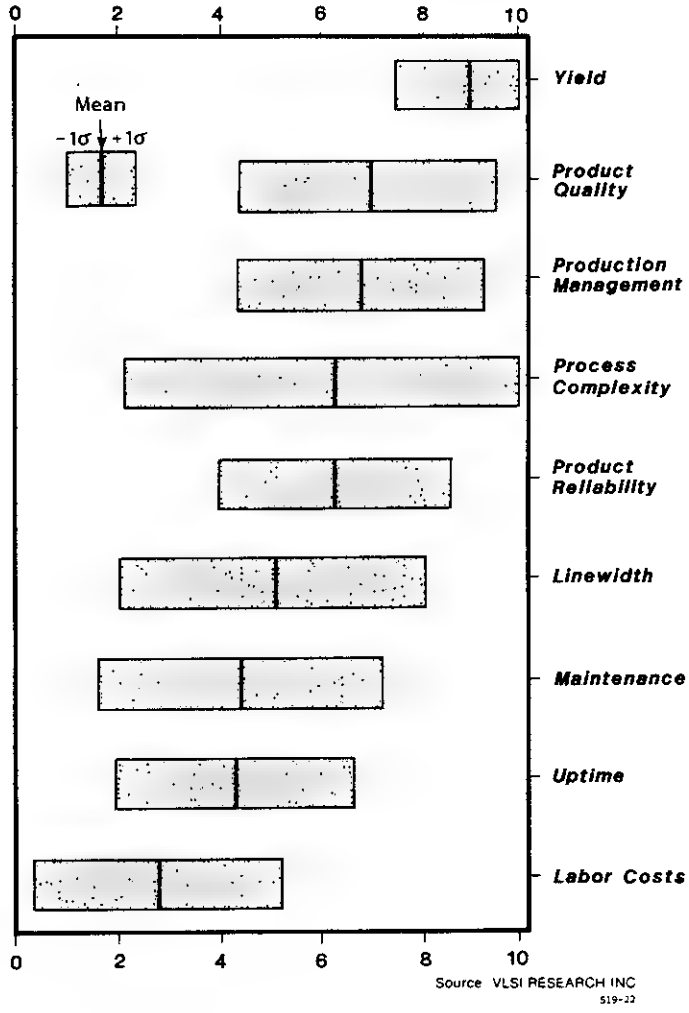
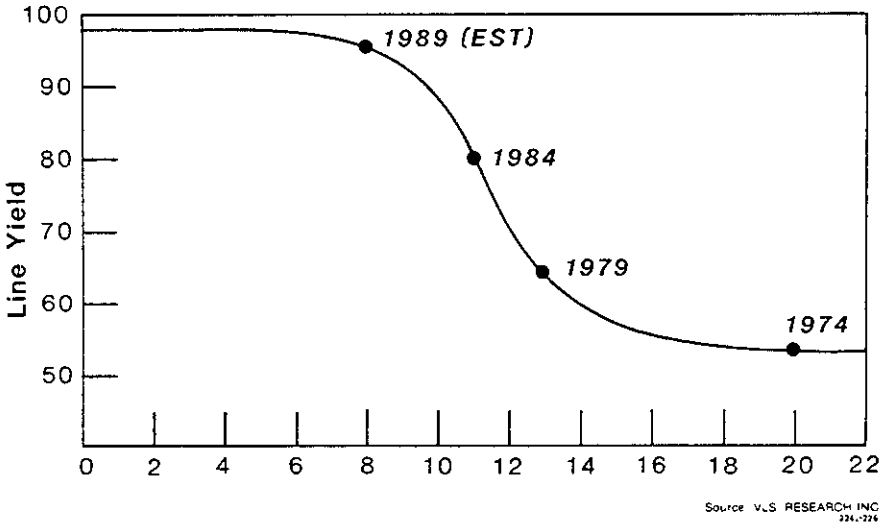


Figure 4.1.2-4

LINE YIELD IMPROVEMENT VERSUS TIME IN PROCESS



Still, the overall cost of automation remains an important issue. As technological advancement slows, the mere reduction of linewidths will not suffice to maintain a company's competitive edge. Today, the semiconductor industry is spending exponentially more to obtain ever smaller improvements in linewidth. Moreover, the resulting improvement in yield is considerably less than it once was. This implies other productivity means must be found. Automation leads to economies-of-scale and to more efficient utilization. One way to reduce manufacturing costs is to increase plant capacity.

Figure 4.1.2-5 shows manufacturing cost on a per kilobit basis for a typical VLSI production line. It shows costs for both an automated and a non-automated line. Today's typical VLSI non-automated product line is represented by the upper curve. As is shown, a non-automated line does not permit the industry to move cost-effectively from 256K bit DRAMs to 1 megabit DRAMs in a cost effective manner. Automation, however, will produce the leverage needed to accomplish this. Cost for such an automated VLSI production line is depicted along the lower curve. This line would allow quite economic production of one megabit DRAMs.

In mid-1983, another interim solution to automation emerged. It was called the box-fab concept, or the tunnel concept. Currently, it appears to be a solid argument for islands of automation and for transport systems. Figure 4.1.2-6 depicts this concept. Here is how it works: Rather than having a bulk yellow room for lithography, surrounded by other equipment outside in a white room, the lithography room is instead divided into a set of boxes. Each box contains all the equipment required for lithography plus enough to strip and etch, as is shown below the box labeled "Litho-1" in the figure. Each box-fab contains a spin-on coater, an aligner, a developer and a dedicated etch station. It may also contain a dedicated inspection system. Only one operator is permitted inside each box. In this manner, class 10 operations are being achieved.

Lots† move through the system on cassette transports. These achieve better than class 10 operation. The transports move cassettes rather than wafers. Cassettes start their movement in the diffusion area and move into WIP control storage areas. From there they are moved via the transport system to the appropriate aligner level for processing. Then, they move back into WIP control storage again to await implant. Next they return to diffusion and the subsequent mask cycle.

† A lot is defined by VLSI Research Inc. to be a group of several wafers, receiving common processing, whose chips will all become a single product type. Generally it contains two cassettes, or 50 wafers.

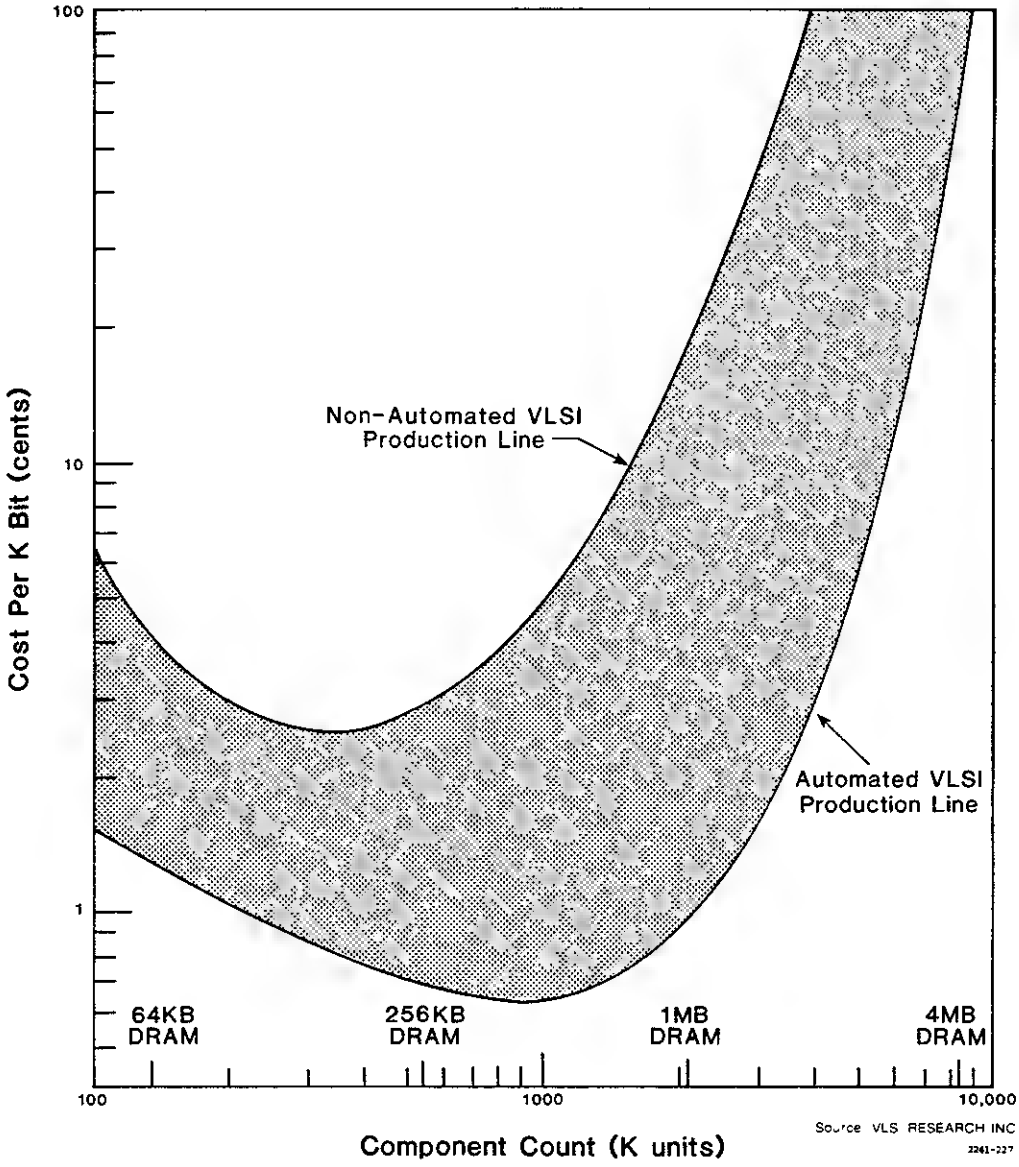


Figure 4.1.2-5

Automation Economics Of Scale

THE BOX FAB CONCEPT

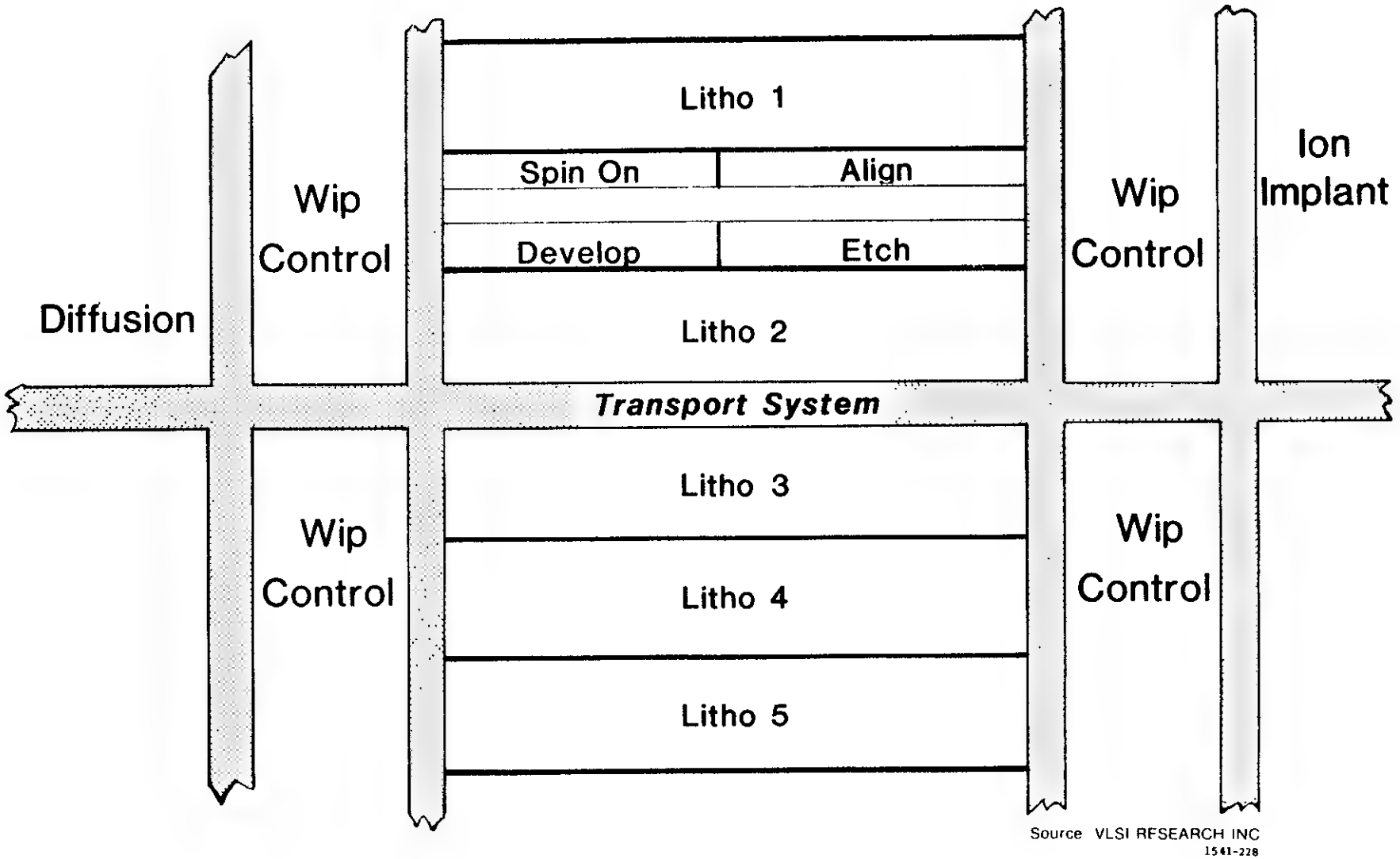


Figure 4.1.2-6

Naturally, not every fab will use the same type of automation. The level of production and flexibility required for each fabrication design will need consideration. Figure 4.1.2-7 shows user preference by type of automation.

It is also expected that two new types of fabs will emerge: One for the manufacture of custom circuits, and the other for high value commodity ICs. VLSI Research Inc. labels these as:

- The "Cinderella Fab" for custom IC production
- The "Monster Fab" for standard ICs

Cinderella Fabs may be typified as those used in ASIC manufacture. They are designed to process a few lots of many different types of designs. Their owner's objective is to turn customer designs into working devices very quickly. This requires an extreme amount of flexibility. Equipment must be capable of being easily and quickly reconfigured to run new products with low tooling costs.

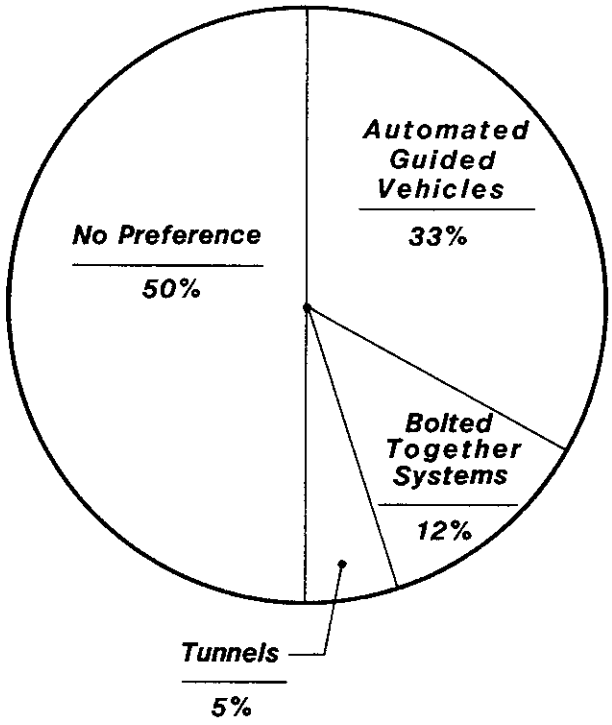
Monster Fabs are typified by those in use by the large merchant semiconductor manufacturers particularly the Japanese, and more specifically, those manufacturing memories. Such large scale plants typically start between 7000 and 10000 wafers per week. Their objective is to produce massive amounts of devices at the lowest possible cost. In the end, Monster Fabs will win large market shares. This is because they produce products at such high volumes that costs quickly move down the manufacturing learning curve. Consequently, major economies of scale are gained. However, competition can be fierce when several companies enter the market, because it only takes a very few (around five or six) to satisfy total world demand.

Despite the economies of scale of monster fab lines, there is increasing evidence they are falling into disfavor. The Japanese installed most of the very largest fab lines—those at or above 7000 wafer starts per week—during the early eighties when they were pushing for world market share dominance. During the severe down-turn of 1985, these fab lines were found to be far too inflexible and could not be converted for use to manufacture other product types. Many Japanese semiconductor suppliers now claim they will return to the less-economical factory sizes of between 2500 and 4000 wafer starts per week.

This failure in automation does not auger well for automation suppliers, for it brings back the specter of inflexibility that users so feared when equipment suppliers first began to delve into automation. Users feel that automation could be better put to use in improving processes and

Figure 4.1.2-7

Preference For Automated Inter-Tool Material Transport



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process yield. Some of the points made are for the equipment supplier to:

(1) Eliminate operator handling of wafers.

(2) Eliminate real time operator decisions on wafer-by-wafer basis.

(3) Make sure the tool does not negate (1) and (2).

(4) Make tools intelligent enough to guarantee a controlled output.

(5) Interface to communication networks for real time tool status and WIP status.

(6) Have a WIP optimization package.

(7) Have a WIP transport system.

(8) Obtain expert systems to assist in problem resolution.

The final need concerns contamination control. Manufacturers should aim for zero particles, of a size greater than one micron, added to wafers during handling and processing. Contamination is a significant threat and is feared by users. End users fear that equipment contamination could replace people contamination in level of importance. Presently, any equipment that rubs, waves, walks or flaps gives off metal flakes. Moreover, if it bumps wafers, it creates silicon dust, as well. Hence, transport systems become trashport systems. Vendors must eliminate this contamination issue. While a start has been made, and several suppliers now specify particles per wafer pass to fewer than 20, still, there is need for substantially greater improvement. One of the methods in current use is to use plastic coated aluminum, called Tufram™, rather than stainless steel.†

† Tufram is a trademark of General Magnaplate.

4.1.4 Competitive Environment in Wafer Fab Equipment

More than 200 companies participate in the wafer fabrication market. The companies range in size from giant companies to very small ones. Collectively, their sales reached $3.1B in 1984, $4.5B in 1988, and can be expected to pass $9.0B around 1993. The drastic downturn following the 1984 peak was not felt in wafer fab equipment until 1986, when annual sales bottomed out at $2.6B.

A list of all major competitors is given in Section 4.1.9. The list is segregated by market served, and is kept current. Nikon ranks number one in wafer fab, having displaced Perkin-Elmer in 1987. Perkin-Elmer had consistently been at the top of the market since inception of top-10 rankings in the VLSI Manufacturing Outlook in 1980. In 1984, Perkin-Elmer's sales were the first to break the quarter billion dollar mark, reaching $269.2M. In 1988, Nikon's sales were the first to break one half billion dollars.

GCA held the number two spot competitively until 1986, having held 6.9% of the total market in 1984. However, GCA spent most of 1986 on the edge of bankruptcy, staying just clear of the need for filing for Chapter 11. GCA was eventually rescued and acquired by General Signal. It has been unclear for some time if they will be able to regain their former spot.

Other major companies are Canon, General Signal, Applied Materials, ASM and TEL.

Japanese firms continued to gain equipment market share in the mid eighties, as was expected. In 1984 their overall wafer fab equipment market share stood at 31%. By 1986 it had improved to 34%. In 1988 it stood at 49%.

There are fourteen major Japanese wafer fabrication equipment suppliers. They are: Canon, Nikon, Nissan High Voltage, TEL, Kokusai, Ulvac, Tokyo Ohka, Anelva, Tokuda Seisakusho, Hitachi, Toshiba, JEOL, Nihon Jido Seigyo and Dainippon Screen. There are eight major European suppliers: ASM, ASM Lithography, Balzers, Cambridge, ET Electrotech, Leybold Heraeus, Riber, and Karl Suss. These and other foreign suppliers jointly supply 50% of total equipment, by value, in 1988. More than one hundred United States firms supplied the remainder.

While American suppliers dominated the market for wafer fabrication equipment through 1986, their overall share was down to 56.5% of the total market by 1986. This represented a 20.5% loss in market share since 1979. By 1988 it had dropped to 50%. Changes in distribution of sales, by market segment and demography, are shown in Table 4.1.4-1 for the years 1984 and 1986. Changes by all segments, for 1983 and 1988 are shown in Table 4.1.4-2.

Europe's renewed strengths have come from government supported projects to keep Europe in the semiconductor industry. Great Britain has the Alvey project. Germany, The Netherlands, Philips & Siemens are supporting a joint effort to produce a 4M bit DRAM. Additionally, German semiconductor manufacturers are participating in a cooperative effort to implement X-ray lithography. This is taking place at the Fraunhofer Institute for Microstructure Technology in Berlin, where a compact synchrotron source (COSY) is being built.

TABLE 4.1.4-1

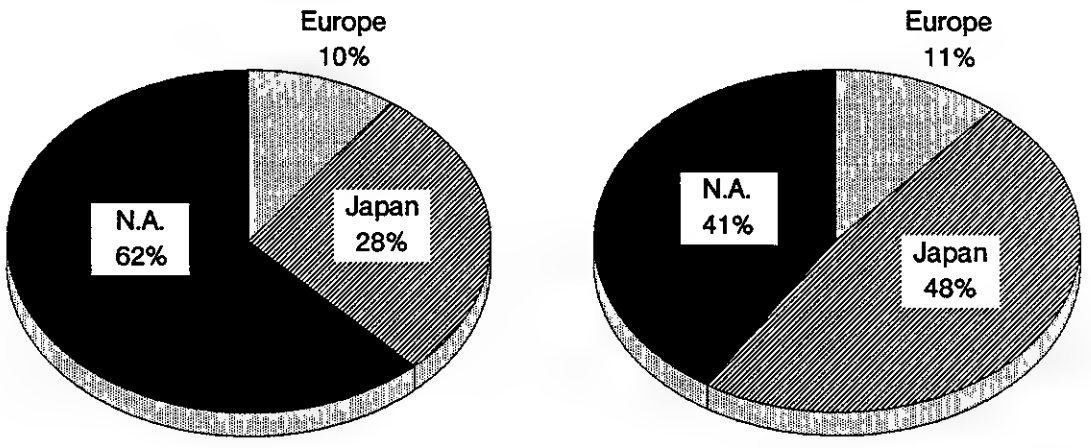
DEMOGRAPHIC DISTRIBUTION OF WAFER FAB SALES

(by percent of seller's shipments, worldwide)

Equipment Type	*United States*		*Japan*		*Europe*	
	1984	*1986*	*1984*	*1986*	*1984*	*1986*
Microlithography & Mask Making	53.3	49.6	43.2	42.0	3.5	8.4
Diffusion/Oxidation	58.6	55.4	36.4	39.2	5.0	5.4
Ion Implantation	74.2	64.3	25.8	35.7	0.0	0.0
Deposition	58.3	53.0	23.5	26.6	18.2	20.4
Etch & Clean	76.7	70.7	20.1	25.6	3.2	3.7
Wafer Manufacturing	80.0	80.0	15.0	15.0	5.0	5.0
TOTAL	61.9	56.5	31.8	33.5	6.3	10.0

TABLE 4.1.4-2

OVERALL WAFER FAB EQUIPMENT MARKET SHARE



4.1.9 Wafer Fab Equipment Database

Section 4.1.9 provides a listing of competitors in the wafer fabrication equipment market. Current competitive data for these companies is provided in each of the following sections:

4.3.9 Microlithography and Mask Making
4.4.9 Diffusion and Oxidation
4.5.9 Ion Implantation
4.6.9 Deposition
4.7.9 Etch and Clean
4.8.9 Wafer Manufacturing

The most recent projections for each market are give in Section 1.9.5 of Volume 1.

TABLE 4.1.9-1

MAJOR SUPPLIERS OF WAFER FABRICATION EQUIPMENT

Company	Lithography & Mask Making	Diffusion/ Oxidation	Ion Implant	Deposition	Etching & Cleaning	Crystal Growing & Machining
Adtex	-	-	-	-	•	-
Advanced Crystal Sciences	-	•	-	•	-	-
AG Associates	-	•	-	-	-	-
Air Control	-	-	-	-	•	-
Alcantech	-	-	-	-	•	-
Amaya	-	-	-	•	-	-
Americhem Engineering	-	-	-	-	•	-
Anelva	-	-	-	•	•	-
Applied Materials	-	-	•	•	•	-
APT	-	-	-	-	•	-
ASET	•	-	-	-	-	-
ASM	-	•	-	•	-	-
ASM Lithography	•	-	-	-	-	-
Astro	-	-	-	-	-	•
Atcor	-	-	-	-	•	-
ATEQ	•	-	-	-	-	-
Atmosphere Control Products	-	-	-	-	•	-
Automated Electronic Tech.	-	•	-	-	-	-
Balzers	-	-	•	•	•	-
Bosch Engineering	-	-	-	•	-	-
Bruce International	-	•	-	•	-	-
Cambridge Instruments	•	-	-	•	-	•
Canon	•	-	-	-	•	-
CHA	-	-	-	•	-	-
Chuo Riken	•	-	-	-	-	-
CIT-Alcatel	-	-	-	•	•	-
CM Inc.	-	-	-	-	-	•
Commonwealth Scientific	-	-	-	•	•	-
Cone Blanchard Machine	-	-	-	-	-	•
Convac	•	-	-	-	-	-
Cooke Vacuum Products	-	-	-	•	•	-
Crystal Mark	-	-	-	-	-	•
Crystal Specialties	-	-	-	•	-	-
CVC	-	-	-	•	-	-
CVD Equipment	-	•	-	•	-	-
Cryogenic & Vacuum Tech.	-	-	-	•	-	-
Cybeq Systems	-	-	-	-	•	•
Daiichi Seiki	-	-	-	-	-	•
Dainippon Screen	•	•	-	-	•	-
DEA Equipment	-	-	-	-	•	-

TABLE 4.1.9-1

MAJOR SUPPLIERS OF WAFER FABRICATION EQUIPMENT

Company	Lithography & Mask Making	Diffusion/ Oxidation	Ion Implant	Deposition	Etching & Cleaning	Crystal Growing & Machining
Denkoh Co. Ltd.	-	•	-	•	-	-
Depositions Systems Europe	-	-	-	•	-	-
Dexon	-	-	-	-	•	-
Disco Abrasive Systems	-	-	-	-	-	•
Drytek	-	-	-	-	•	-
Dynapert/Precima	•	-	-	-	-	-
Eagle Technologies	-	-	-	-	•	-
Eaton	•	•	•	•	•	-
Eaton/Sumitomo	-	-	•	-	-	-
Eiko Engineering	-	-	-	•	-	-
Electric Arc	-	-	-	-	-	•
Elionixs	•	-	-	-	-	-
Emcore	-	-	-	•	-	-
Emergent Technologies	-	-	-	-	•	-
Emerson Electric	-	-	-	-	•	-
ET Electrotech	-	-	-	•	•	-
Focus Semiconductor Systems	-	-	-	•	-	-
FSI	-	-	-	-	•	-
Fuji	•	-	-	-	-	-
Fuji Advanced Corp.	-	-	-	-	•	-
Fujikoshi	-	-	-	-	-	•
Fusion Semiconductor	•	-	-	-	-	-
Gasonics	•	•	-	-	•	-
Gemini Research	-	-	-	•	-	-
General Diode	-	-	-	-	-	•
General Signal	•	•	-	•	•	•
Genus	-	-	•	•	-	-
Geos Corporation	-	-	-	-	-	•
Grinding Technology	-	-	-	-	-	•
H & L Instruments	-	-	-	-	-	•
Headway Research	•	-	-	-	-	•
Helmut Seier	-	•	-	-	-	-
Hitachi, Ltd.	•	-	•	•	•	•
Hitachi Seiko	-	-	-	-	-	•
Hybrid Technology Group	•	-	-	-	-	-
Imnotech	-	-	-	•	-	-
Institute for Electronics	•	-	-	-	-	-
Integrated Air Systems	-	-	-	-	•	-
Interlab	-	-	-	-	•	-
Irie Koken	-	-	-	•	-	-

TABLE 4.1.9-1

MAJOR SUPPLIERS OF WAFER FABRICATION EQUIPMENT

Company	Lithography & Mask Making	Diffusion/ Oxidation	Ion Implant	Deposition	Etching & Cleaning	Crystal Growing & Machining
Irie Siesakusho	•	-	-	-	-	•
Japan Electronic Prod. Engrg.	-	-	-	•	-	-
Jenoptik Jena	•	-	-	-	-	-
JEOL	•	-	-	-	-	•
Kaijyo Denki	•	-	-	-	•	-
Karl Suss	•	-	-	-	-	-
Kitano Seini	-	-	-	•	-	-
Kokusai Electric	-	•	-	•	•	•
Koyo Lindberg	-	•	-	•	-	-
Lam Research	-	-	-	-	•	-
Lapmaster	-	-	-	-	-	•
Laser Technology	-	-	-	-	-	•
Lepel Corporation	-	-	-	-	-	•
Leybold-Heraeus	-	-	-	•	-	•
LFE	-	-	-	-	•	-
Logitech	-	-	-	-	-	•
M. Setek	•	-	-	-	-	-
Machine Technology Inc.	-	-	-	•	•	-
Materials Research Corp.	-	-	-	•	•	-
Matrix	-	-	-	-	•	-
Matsushita	-	•	-	-	-	-
Meyer & Burger	-	-	-	-	-	•
MicroAir Manufacturing Inc.	-	-	-	-	•	-
Microbeam	•	-	-	-	-	-
Mitsui Bissan	•	-	-	-	-	-
MRS	•	-	-	-	-	-
M. Watanabe & Co.	-	-	-	-	•	-
Nagase	•	-	-	-	-	-
Nanosil	-	-	-	•	-	-
National Electrostatics	-	-	•	-	-	-
NEC	-	•	-	-	-	-
Nikon	•	-	-	-	-	-
Nippon Bietec	-	-	-	•	-	-
Nippon Sanso	-	-	-	•	-	-
Nippon Seikosho	•	-	-	-	-	-
Nippon Seisan Gijutsu Kenkujo	-	-	-	•	-	-
Nissin Electric Co.	-	-	•	-	-	-
Novellus	-	-	-	•	-	-
Okamato	-	-	-	-	-	•
Optical Radiation	•	-	-	-	-	-

TABLE 4.1.9-1

MAJOR SUPPLIERS OF WAFER FABRICATION EQUIPMENT

Company	Lithography & Mask Making	Diffusion/ Oxidation	Ion Implant	Deposition	Etching & Cleaning	Crystal Growing & Machining
Oxford Instruments	-	-	-	-	•	-
P.R. Hoffman	-	-	-	-	-	•
Pacific Western Systems	-	•	-	•	-	-
Peak Systems	-	•	-	-	-	-
Perkin Elmer	•	-	-	•	-	-
Peter Wolters of America	-	-	-	-	-	•
Phoenix Materials	-	-	-	•	-	-
Plasma Physics	-	-	-	•	-	-
Plasma Systems	-	-	-	-	•	-
Plasma Technology	-	-	-	•	•	-
Plasma-Therm	-	-	-	•	•	-
Polyflow Engineering	-	-	-	-	•	-
Presi SA	-	-	-	-	-	•
Probe Rite	•	-	-	-	-	-
Process Products	-	•	-	-	-	-
Process Technology	-	-	-	•	-	-
Pure Aire	-	-	-	-	•	-
Quantronix	-	•	-	-	-	-
Reid Ashman	-	-	-	-	•	-
Riber	-	-	-	•	-	-
Samco	-	-	-	•	-	-
SCP Manufacturing	-	-	-	-	•	-
Helmut Seier	-	•	-	-	-	-
Seinan Kogyo	-	-	-	•	-	-
Semco	-	-	-	-	-	•
Semiconductor Eng. Labs	-	-	-	•	-	-
Semifab	-	-	-	-	•	-
Semitherm	-	•	-	-	-	-
Semy Engineering	-	-	-	•	-	-
Shimada Rika Kogyo	-	-	-	•	•	-
Shinko Seiki	-	-	•	-	-	-
Sigma Engineering	-	-	-	-	•	-
Silicon Valley Group	•	•	-	•	•	•
Silicon Technology	-	-	-	-	-	•
SIMCO International Ltd.	-	-	-	-	-	•
Solitec	•	-	-	-	-	-
SPC	-	-	-	•	-	-
Spectrum CVD	-	-	-	•	-	-
Speedfam Corporation	-	-	-	-	-	•
Spire	-	•	-	•	-	-

TABLE 4.1.9-1

MAJOR SUPPLIERS OF WAFER FABRICATION EQUIPMENT

Company	Lithography & Mask Making	Diffusion/ Oxidation	Ion Implant	Deposition	Etching & Cleaning	Crystal Growing & Machining
Spitfire Tool & Machine	-	-	-	-	-	•
Sputtered Films Inc.	-	-	-	•	-	-
Stanelco	-	-	-	-	-	•
R. Howard Strasbaug Inc.	-	-	-	-	-	•
Sumitomo	-	-	-	•	-	-
Tamarack	•	•	-	-	-	-
Tanaka Systems	-	-	-	-	-	•
Tazmo	•	-	-	-	-	-
Techmashexport	•	-	-	-	-	-
Tegal	-	-	-	-	•	-
Tokyo Electron Ltd.	•	•	•	•	•	-
Temescal (BOC)	-	-	-	•	•	-
The Semi Group	-	-	-	•	•	-
Timesa Microelectronics	-	-	-	•	-	-
Tokuda Seisakusho	-	-	-	•	•	-
Tokyo Ohka	•	-	-	-	•	-
Tokyo Seimitsu (TSK)	-	-	-	-	-	•
Toshiba	•	-	-	•	-	•
Toyoka Kagaku	-	-	-	•	-	-
Trebor	-	-	-	-	•	-
Tylan	-	•	-	•	-	-
Ulvac	-	•	•	•	•	-
Ulvac/BTU	-	•	-	-	-	-
Unitra	-	•	-	-	-	-
Ushio	-	•	-	-	-	-
Varian	-	•	•	•	•	-
Veeco	•	-	•	•	•	-
Vertag	-	-	-	-	•	-
VG Semicon	-	-	-	•	-	-
Watkins-Johnson	-	-	-	•	-	-
Wellman Furnaces	-	•	-	-	-	•
Westech	-	-	-	-	-	•
Western Technology Assoc.	-	-	-	-	•	-
William Dixon	-	-	-	-	-	•
Xennon	-	-	-	-	•	-
Yamato	-	-	-	-	•	-

Source: VLSI RESEARCH INC
2202-361W

Notes